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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/800,048
Filing Date: March 11, 2004
Appellant(s): STENFORT ET AL.

MAILED

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Technology Center 2100

Kenneth D. Wright
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 7/25/2007 appealing from the Office action mailed on 11/14/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

20050188123	Chen et al	Aug 25, 2005
20040137952	Umesh et al	July 15, 2004

20040019432	Sawafta et al	Jan 29, 2004
20050089012	Martin et al	April 28, 2005

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5, 6, 9, 11, 12, 13, 14, 18, 20 are rejected under 103(a) as being unpatentable over Chen (US Patent Application Publication 2005/0188123), in view of Umesh et al (US Patent Application No. 2004/0137952).

For claim 1, Chen teaches the following limitations:

An apparatus for controlling an alignment signal transmission ([0008] mentions that a system and method for inserting Interval Markers in a data stream is provided. Interval Markers are alignment signal, since they do not represent data but are required for data flow management) **in an electronic communication process** (100), **comprising: a counter** (buffer count BC in Fig 6) **configured to sequentially modify**

a count value in accordance with an associated clock signal (BC changes with respect to clock as explained in [0059]. Fig 6 shows the steps of changing BC. Thus, BC changes sequentially); **a storage cell configured to** (MO in Fig 6) **receive and store an alignment trigger value** ([0010] mentions that MO counter indicates the next location for insertion of Marker. Thus, MO stores alignment trigger value that triggers the system to insert alignment signal); **a comparator connected to receive the count value as an input from the counter and the alignment trigger value as an input from the storage cell, the comparator configured to compare the count value to the alignment trigger value** ([0059] mentions that BC and MO are compared with each other, which requires a comparator), **the comparator further configured to send an output signal from an output port upon comparison of the count value and the alignment trigger value** ([0059] mentions that an Interval Marker is inserted at clock cycle 2 when BC is greater than MO. Therefore, contents of registers shown in Fig 4 are rearranged based on comparison between MO and BC. Thus, comparison sends a signal to the system to rearrange the registers 402. [0049] shows comparison includes equivalence condition); **and alignment circuitry** (402 and part of 308 that generate and insert Marker FF) **connected to receive the output signal from the comparator** (contents of registers 402 shown in Fig 4 are rearranged upon based on comparison between MO and BC. Thus, comparison sends a signal to the system to rearrange the registers 402), **the alignment circuitry configured to generate and transmit an alignment signal to a target transceiver** (FF in Fig 6 is the alignment signal is transmitted to target system 104 with data) **in response to receipt of the output**

signal from the comparator (FF is inserted when BC is greater than MO. [0056]-[0058] and [0049]. The transmission occurs after the insertion of Marker in proper place. Thus, alignment signal is generated and transmitted in response to comparison between BC and MO), **wherein the alignment signal represents a dword** (FF is a dword) **to be ignored by internal logic of the target transceiver** (FF does not represent data. It only represents the boundary. Therefore, it is ignored in the data processing operation in target transceiver).

Although Chen compares count value with alignment trigger value and conditionally inserts Marker when BC=MO ([0056] mentions 514 state is for insertion of Marker and [0049] provides condition for transition to 514 that includes BC=MO), Chen's system also inserts Marker when BC and MO are not equal and Chen system sometimes does not insert marker for BC=MO. Although claim does not preclude generation of alignment signal when count value not equal to alignment value and does not require unconditional generation of alignment signal whenever BC=MO, Examiner cites Umesh et al to show the generation of alignment signal based on equivalence of count value and alignment trigger value.

Umesh et al teach the following limitations:

a storage cell configured to receive and store an alignment trigger value (16);a comparator (14) connected to receive the count value as an input from the counter (Fig 5) and the alignment trigger value as an input from the storage cell (16), the comparator configured to compare the input from the counter to

the input from the storage cell (Fig 5), the comparator further configured to send an output signal from an output port upon equivalence of the input from the counter and the input from the storage cell (output of 14 is the input to 15); and alignment circuitry (combination of 11, 12 and 15) connected to receive the output signal from the comparator (15 receives output from 14), the alignment circuitry configured to generate and transmit an alignment signal (the directional beam generated according to antenna weight can be thought as an alignment signal, since it is used to align base station with mobile station) through an initiator transceiver (base station) to a target transceiver (mobile station) in response to receipt of the output signal from the comparator (the output of 14 is used to generate appropriate antenna weight that is used to adjust directional beam).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine Chen and Umesh. One ordinary skill in the art would be motivated to have a comparator to compare count value with alignment trigger value and send output upon equivalence of count value with the alignment trigger value, since that depends on the design choice of the designer. Chen considers the equivalence criteria but it is not the sole criteria. One ordinary skill can choose a different design where alignment signal is generated upon equivalence of counter and trigger value.

For claim 3, BC counter of Chen resets to a new value and restarts counting when new data is loaded to 402 or data is transmitted from 402. Both operation depends on

Marker Insertion, which itself depends on comparison. Therefore, a signal from comparator is used to signal Block Counter to reset and restart when appropriate.

For claim 5, the process happens in initiator transceiver of Chen.

For claim 6, alignment trigger value MO has a component that represents number of transmission unit to be transmitted between each interval transmission ([0043] mentions MO depends on MI, which is the Marker Interval. Marker interval represents data transmission unit between alignment signal transmission).

For claim 9, Chen teaches the following limitations:

A method for controlling an alignment signal transmission ([0008] mentions that a system and method for inserting Interval Markers in a data stream is provided. Interval Markers are alignment signal, since they do not represent data but are required for data flow management) **in an electronic communication process** (100), **comprising:**

selecting an alignment trigger value ([0010] mentions that MO counter indicates the next location for insertion of Marker. Thus, MO stores alignment trigger value that triggers the system to insert alignment signal);

operating a counter (buffer count BC in Fig 6) **to sequentially modify a count value in accordance with an associated clock signal** (BC changes with respect to clock as explained in [0059]);

transmitting from an initiator transceiver to a target transceiver an alignment signal in place of transmission unit (FF is transmitted from 102 to 104) **when count**

value equals the alignment trigger value ([0059] mentions that an Interval Marker is inserted at clock cycle 2 as BC is greater than MO. [0056]-[0058] and [0049]. The transmission occurs after the insertion of Marker in proper place. Thus, alignment signal is generated and transmitted in response to equivalence between BC and MO. [0049] shows comparison includes equivalence condition), **wherein the alignment signal represents a dword to be ignored by internal logic of the target transceiver** (FF does not represent data. It only represents the boundary. Therefore, it is ignored in the data processing operation in target transceiver).

Although Chen compares count value with alignment trigger value and conditionally inserts Marker when BC=MO, Chen's system also inserts Marker when BC and MO are not equal (Chen system sometimes does not insert marker for BC=MO). Although claim does not preclude generation of alignment signal when count value not equal to alignment value and does not require unconditional generation of alignment signal when BC=MO, Examiner cites Umesh et al that generate alignment signal based on equivalence of count value and alignment trigger value.

Umesh et al teach the following limitations:

a storage cell configured to receive and store an alignment trigger value (16);a comparator (14) connected to receive the count value as an input from the counter (Fig 5) and the alignment trigger value as an input from the storage cell (16), the comparator configured to compare the input from the counter to

the input from the storage cell (Fig 5), the comparator further configured to send an output signal from an output port upon equivalence of the input from the counter and the input from the storage cell (output of 14 is the input to 15); and alignment circuitry (combination of 11, 12 and 15) connected to receive the output signal from the comparator (15 receives output from 14), the alignment circuitry configured to generate and transmit an alignment signal (the directional beam generated according to antenna weight can be thought as an alignment signal, since it is used to align base station with mobile station) through an initiator transceiver (base station) to a target transceiver (mobile station) in response to receipt of the output signal from the comparator (the output of 14 is used to generate appropriate antenna weight that is used to adjust directional beam).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine Chen and Umesh. One ordinary skill in the art would be motivated to have a comparator to compare count value with alignment trigger value and send output upon equivalence of count value with the alignment trigger value, since that depends on the design choice of the designer. Chen considers the equivalence criteria but it is not the sole criteria. One ordinary skill can choose a different design where alignment signal is generated upon equivalence of counter and trigger value.

For claim 11, trigger value of Chen can be any value.

For claims 12 and 13, [0049] of Chen shows the comparison. A comparator implementing comparison is therefore present.

For claim 14, BC counter of Chen resets to a new value and restarts counting when new data is loaded to 402 or data is transmitted from 402. Both operation depends on Marker Insertion, which itself depends on comparison. Therefore, a signal from comparator is used to signal Block Counter to reset and restart when appropriate.

For claim 18, Chen teaches the following limitations:

A computer readable media containing program instructions for controlling alignment signal transmission ([0008] mentions that a system and method for inserting Interval Markers in a data stream is provided. Interval Markers are alignment signal, since they do not represent data but are required for data flow management) **in an electronic communication process** (100), **comprising:**

program instruction for selecting an alignment trigger value ([0010] mentions that MO counter indicates the next location for insertion of Marker. Thus, MO stores alignment trigger value that triggers the system to insert alignment signal);

program instructions for sequentially modifying a count value (BC changes with respect to clock as explained in [0059]);

program instructions for transmitting from an initiator transceiver to a target transceiver an alignment signal in place of transmission unit (FF is transmitted

from 102 to 104) **when count value equal to the alignment trigger value** ([0059] mentions that an Interval Marker is inserted at clock cycle 2 as BC is greater than MO. [0056]-[0058] and [0049]. The transmission occurs after the insertion of Marker in proper place. Thus, alignment signal is generated and transmitted in response to equivalence between BC and MO. [0049] shows comparison includes equivalence condition), **wherein the alignment signal represents a dword to be ignored by internal logic of the transceiver** (FF does not represent data. It only represents the boundary. Therefore, it is ignored in the data processing operation in target transceiver).

Although Chen compares count value with alignment trigger value and conditionally inserts Marker when BC=MO, Chen's system also inserts Marker when BC and MO are not equal (Chen system sometimes does not insert marker for BC=MO). Although claim does not preclude generation of alignment signal when count value not equal to alignment value and does not require unconditional generation of alignment signal whenever BC=MO, Examiner cites Umesh et al that generate alignment signal based on equivalence of count value and alignment trigger value.

Umesh et al teach the following limitations:

a storage cell configured to receive and store an alignment trigger value (16);a comparator (14) connected to receive the count value as an input from the counter (Fig 5) and the alignment trigger value as an input from the storage cell (16), the comparator configured to compare the input from the counter to

the input from the storage cell (Fig 5), the comparator further configured to send an output signal from an output port upon equivalence of the input from the counter and the input from the storage cell (output of 14 is the input to 15); and alignment circuitry (combination of 11, 12 and 15) connected to receive the output signal from the comparator (15 receives output from 14), the alignment circuitry configured to generate and transmit an alignment signal (the directional beam generated according to antenna weight can be thought as an alignment signal, since it is used to align base station with mobile station) through an initiator transceiver (base station) to a target transceiver (mobile station) in response to receipt of the output signal from the comparator (the output of 14 is used to generate appropriate antenna weight that is used to adjust directional beam).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine Chen and Umesh. One ordinary skill in the art would be motivated to have a comparator to compare count value with alignment trigger value and send output upon equivalence of count value with the alignment trigger value, since that depends on the design choice of the designer. Chen considers the equivalence criteria but it is not the sole criteria. One ordinary skill can choose a different design where alignment signal is generated upon equivalence of counter and trigger value.

For claim 20, trigger value can be any value.

Claims 2, 10, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, in view of Umesh et al (US Patent Application Publication 2004/0137952), further in view of Sawafta et al (US Patent Application Publication 2004/0019432).

For claims 2, 10, 19, Chen, in view of Umesh et al do not explicitly mention that the threshold can be set through user interface. Sawafta et al's system sets trigger value through interface ([0058]).

One ordinary skill in the art would be motivated to change the system of Chen, in view of Umesh et al to set trigger through user interface, since that provide the flexibility of setting the threshold. Chen also suggests setting trigger ([0043] shows MO depends on MI and [0031] discusses setting of MI).

Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, Umesh et al (US Patent Application Publication 2004/0137952), in view of Martin et al (US Patent Application Publication 2005/0089012).

Chen or Umesh et al do not teach any delay circuit to compensate latency. Martin et al teach delay circuit to compensate latency ([0046] of page 4).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine Chen, Umesh et al and Martin et al. One ordinary skill in the art would have been motivated to compensate latency by including a delay circuit, since that would ensure accuracy.

Claims 7, 8, 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, in view of Umesh et al (US Patent Application Publication 2004/0137952), further in view of AAPA (Applicant's Admission of Prior Art).

For claims 7 and 16, Chen or Umesh et al do not explicitly mention that the communication process is performed in accordance to SAS or SATA protocol. Chen mentions that SATA is well known in the art ([0004]). One ordinary skill in the art would be motivated to implement the system of Chen, in view of Umesh et al in accordance to SAS or SATA, since SCSI and AT devices allows a number of peripheral devices to be attached. Chen system allows other specifications to be used ([0061]) besides SCSI. About dword and ALIGN primitive, applicant admits that these are requirements of SATA (lines 12-14 of page 8).

For claims 8 and 17, Chen teaches PHY.

Response to Arguments

Appellant's arguments filed on 7/25/2007 have been fully considered but they are not persuasive.

Appellant argues that the cited art does not teach generation and transmission of an alignment signal that represents a dword to be ignored by internal logic of a target transceiver. As interval markers provide information on how many bytes to skip in the TCP stream in order to find the next iSCSI PDU header and the fixed interval markers are required at fixed intervals for data flow management, the interval markers of Chen are in fact processed by the target transceiver in a data transmission scheme in order to extract the data for locating PDU headers to enable management of data flow.

Examiner acknowledges that markers are required for data flow management and markers provide information on how many bytes to skip in the TCP stream to find the next header. The claim requires "dword to be ignored by internal logic of target transceiver", instead of "dword that is not processed by the receiver". Before whether or not the markers in Chen are ignored by the internal logic of the target transceiver, the examiner would like to revisit the disclosure see how dword is ignored by the target transceiver in appellant's own invention.

According to the specification, an alignment signal is inserted in the dword stream for clock management ([0018] of page 5). The alignment signal can be one of eight

primitives. The insertion of the alignment signal serves to delay transmission of dword stream which consequently allows the receiver to avoid an overrun condition. Thus, the receiver has to distinguish between the alignment signal and the stream content that must be processed by the internal logic of the receiver. Making this distinction between the alignment signal and the stream content requires processing within the receiver, since receiver has to understand what to ignore and what to process. Therefore, although the alignment signal is ignored during further processing, the alignment signal is initially processed to check whether it is part of the stream content.

The interval markers in Chen are for data flow management ([0011]). The interval markers are inserted between data blocks ([0010]). Figure 2 shows a PDU where markers 218, 220, 222 and 224 are inserted. From Figure 2, it is clear that the markers are not part of data. From iSCSI specification, we know that markers indicate how many bytes to skip in the TCP stream in order to find the next iSCSI PSU header. Thus, the purpose of the markers, as indicated by their name, is to point to the location of the next iSCSI PSU header. Therefore, the part of the receiver responsible for data blocks processing does not need to process the marker since the marker is not part of data blocks. Once PDU header is located, the markers are ignored by the internal logic of the receiver. The logic of receiver that is responsible for processing data blocks, does not need to process the markers since the markers are not part of data blocks.

Appellant further argues that the cited art does not teach a counter to sequentially modify a count value in accordance with an associated clock signal.

Paragraphs [0033]-[0060] of Chen describe how the BC is modified in accordance with the clock. Figure 6 shows how the BC is operated to modify a count value in accordance with a clock signal. This modification is a sequential modification as discussed below:

Figure 5 shows the state machine governing the operation of the system. Paragraphs [0037]-[0043] explain the rules governing modification of counter BC. Considering both Figure 5 and the discussion in paragraphs [0037]-[00430, it becomes apparent that the BC is modified according to some predetermined rule. At clock cycle 0, BC = 0 ([0035]), at clock cycle 1, BC = 4 (i.e., DBin; [0037]), at clock cycle 2, BC = 6 (i.e., follows rule of [0049]), at clock cycle 3, BC = 10 (as BC + DBin <= Q mentioned in [0045]); at clock cycle 4, BC = 4 (i.e., buffer full and data is sent). Thus, the count value of buffer BC follows the sequence of 0, 4, 6, 10 in accordance with clock cycle 0, 1, 2, 3 as long as MO = 3, Q= 10, ML = 2, DBin = 4, DBout = 4. Depending on the parameter values, the same sequence can be followed according to the predetermined rules mentioned in paragraphs [0035]-[0058]. The rules and parameters that control the sequence of the value of the BC allow sequential modification of the count value for at least for some instances, thus meeting the claim limitations.

Appellant further argues that Chen teaches changing the value of the BC in any given single clock cycle by either plus 128 bits, plus 8 bits, or minus 16 bits. Therefore, Chen's teachings with regard to buffer count simply do not teach sequential modification of a count value in accordance with a clock signal.

As explained earlier, Chen's system does not preclude sequential modification of a count value. The count value may be modified sequentially in some instances depending on the rules and parameters. Any desired combination, such as DBin = 4, ML = 2, Q =20, MO = 3, would result in a sequential count value modification such as: 0, 4, 6, 10, 12, 16 according to clock cycle 0, 1, 2, 3, 4, 5.

Appellant further argues that neither Chen nor Umesh provide a motivation or suggestion for one of the ordinary skill in the art to combine the teachings.

Examiner cited Umesh to explain the generation of the alignment signal based on the equivalence of the count value and the alignment trigger value. As Chen already has such teaching (which is not argued by appellant), Umesh need not be relied upon for this teaching. However, the express teachings of Umesh would motivate one of ordinary skill in the art to use a different comparator design.

For the above reasons, it is believed that rejections should be sustained.

Respectfully submitted,

Fahmida Rahman

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Examiner

Art Unit 2116

September 25, 2007

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